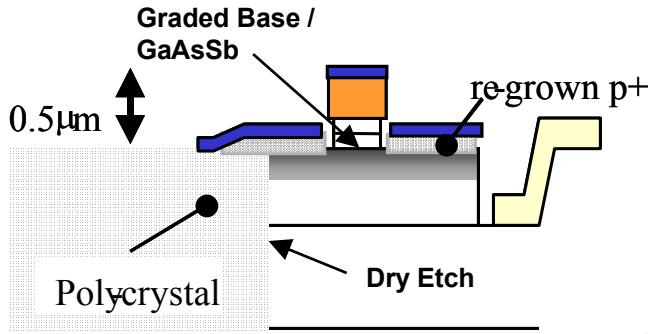
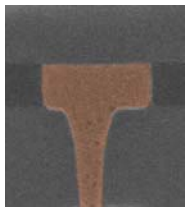
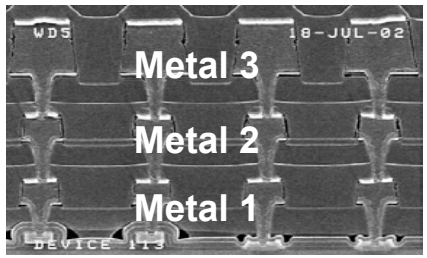
Graphic of Technology







Goals, Objectives and Main Technical Approach

Super-scaled InP HBT device development at UIUC and transition to Vitesse of planar 0.25mm HBTs along with 4 level copper interconnect results in an optimal, high yield, manufacturable process with F_t and F_{max} exceeding 400 GHz, and Flip-Flop performance of 200 GHz exceeding that of any other competing technology. Techniques developed by the silicon industry

Major Technical Accomplishments

(since start of contract)

- *Validated transistor design approach*
- *0.45 um transistors operating*
- *Started topology reduction experiment*
- *Significant design kit progress*
- *Started fab of GaAsSb transistor*

Major Work Remaining to Completion of Contract

- *Develop 0.25 um transistors with multi level interconnect*
- *Develop 150GHz FF*
- *Develop DDS application circuit*

Major Impact of Technology & Technology Transition Plan

Enables a revolutionary combination of :

- *Ultra-high speed performance*
- *High integration levels*
- *Low power dissipation*
- *High Linearity*

In one integrated circuit that is well suited for a future generation of miniaturized, agile, RF transceiver applications incorporating high performance DDS circuits. Transistor development aimed at commercialization by Vitesse from the start using 6” copper process.